



HIGH EFFICIENCY CLASS-G ADSL LINE DRIVER

FEATURES

- **Low Total Power Consumption Increases ADSL Line Card Density (20 dBm on Line)**
 - 600 mW w/Active Termination (Full Bias)
 - 530 mW w/Active Termination (Low Bias)
- **Low MTPR of -74 dBc (All Bias Conditions)**
- **High Output Current of 500 mA (typ)**
- **Wide Supply Voltage Range of ±5 V to ±15 V [V_{CC(H)}] and ±3.3 V to ±15 V [V_{CC(L)}]**
- **Wide Output Voltage Swing of 43 V_{pp} Into 100-Ω Differential Load [V_{CC(H)} = ±12 V]**
- **Multiple Bias Modes Allow Low Quiescent Power Consumption for Short Line Lengths**
 - 160-mW/ch Full Bias Mode
 - 135-mW/ch Mid Bias Mode
 - 110-mW/ch Low Bias Mode
 - 75-mW/ch Terminate Only Mode
 - 13-mW/ch Shutdown Mode
- **Low Noise for Increased Receiver Sensitivity**
 - 3.3 pA/√Hz Noninverting Current Noise
 - 9.5 pA/√Hz Inverting Current Noise
 - 3.5 nV/√Hz Voltage Noise

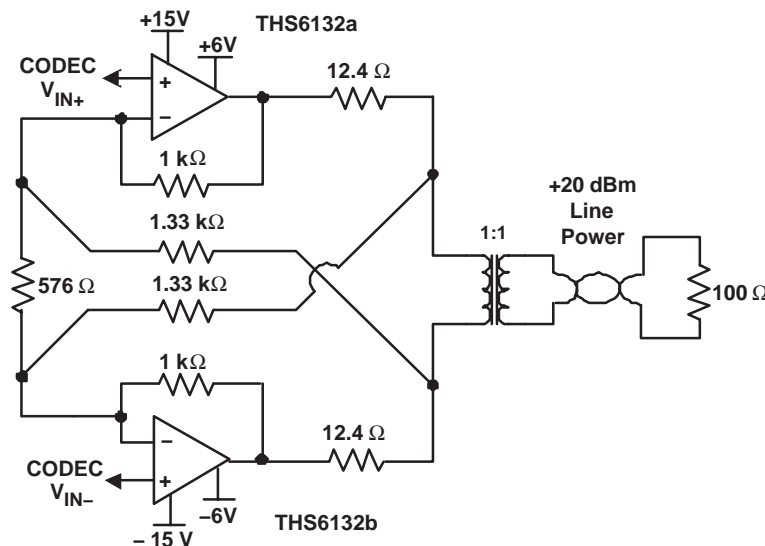
APPLICATIONS

- **Ideal for Active Termination Full Rate ADSL DMT applications (20-dBm Line Power)**

DESCRIPTION

The THS6132 is a Class-G current feedback differential line driver ideal for full rate ADSL DMT systems. Its extremely low power consumption of 600 mW or lower is ideal for ADSL systems that must achieve high densities in ADSL central office rack applications. The unique patent pending architecture of the THS6132 allows the quiescent current to be much lower than existing line drivers while still achieving very high linearity. In addition, the multiple bias settings of the amplifiers allow for even lower power consumption for line lengths where the full performance of the amplifier is not required. The output voltage swing has been vastly improved over first generation Class-G amplifiers and allows the use of lower power supply voltages that help conserve power. For maximum flexibility, the THS6132 can be configured in classical Class-AB mode requiring only as few as one power supply.

Typical ADSL CO Line Driver Circuit Utilizing Active Impedance Supporting A 6.3 Crest Factor



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage.

ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	SYMBOL	T _A	ORDER NUMBER	TRANSPORT MEDIA
THS6132VFP	TQFP-32 PowerPAD™	VFP-32	THS6132	-40°C to 85°C	THS6132VFP	Tube
					THS6132VFP	Tape and reel
THS6132RGW	Leadless 25-pin 5,mm x 5, mm PowerPAD™	RGW-25	6132		THS6132RGWR	Tape and reel

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ _{JA}	Θ _{JC}	T _A ≤ 25°C POWER RATING(1)	T _A = 70°C POWER RATING(1)	T _A = 85°C POWER RATING(1)
VFP-32	29.4°C/W	0.96°C/W	3.57 W	2.04 W	1.53 W
RGW-25	31°C/W	1.7°C/W	3.39 W	1.94 W	1.45 W

(1) Power rating is determined with a junction temperature of 130°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		THS6132
Supply voltage, V _{CC(H)} and V _{CC(L)} (2)		±16.5 V
Input voltage, V _I		±V _{CC(L)}
Output current, I _O (3)		900 mA
Differential input voltage, V _{IO}		±2 V
Maximum junction temperature, T _J (see Dissipation Rating Table for more information)		150°C
Operating free-air temperature, T _A		-40°C to 85°C
Storage temperature, T _{Stg}		65°C to 150°C
Lead temperature, 1,6 mm (1/16-inch) from case for 10 seconds		300°C
ESD ratings	HBM	1 kV
	CDM	500 V
	MM	200 V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) V_{CC(H)} must always be greater than or equal to V_{CC(L)} for proper operation. Class-AB mode operation occurs when V_{CC(H)} is equal to V_{CC(L)} and is considered acceptable operation for the THS6132 even though it is not fully specified in this mode of operation.

(3) The THS6132 incorporates a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature that could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage	+V _{CC(H)} to -V _{CC(H)}	±V _{CC(L)}	±15	±16	V
	+V _{CC(L)} to -V _{CC(L)}	±3.3	±5	±V _{CC(H)}	
Operating free-air temperature, T _A		-40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, T_A = 25°C, V_{CC(H)} = ±15 V, V_{CC(L)} = ±5 V R_F = 1.5 kΩ, Gain = +10, Full Bias Mode, R_L = 50 Ω (unless otherwise noted)

NOISE/DISTORTION PERFORMANCE							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Multitone power ratio		Gain = +11, 163kHz to 1.1MHz DMT, +20 dBm Line Power, 1:1.1 transformer, active termination, synthesis factor = 4			-74		dBc
Receive band spill-over		Gain = +11, 25 kHz to 138 kHz with MTPR signal applied			-95		dBc
HD	Harmonic distortion (Differential Configuration, f = 1 MHz, V _{O(PP)} = 2 V, Gain = +10)	2 nd harmonic	Differential load = 100 Ω		-84		dBc
			Differential load = 25 Ω		-69		
		3 rd harmonic	Differential load = 100 Ω		-92		dBc
			Differential load = 25 Ω		-73		
V _n	Input voltage noise	f = 10 kHz			3.5		nV/√Hz
I _n	Input current noise	+Input	f = 10 kHz			3.3	pA/√Hz
		-Input				9.5	
Crosstalk		f = 1 MHz, R _L = 100 Ω,	V _{O(PP)} = 2 V, Gain = +2		-52		dBc
OUTPUT CHARACTERISTICS							
V _O	Single-ended output voltage swing	V _{CC(H)} = ±12 V	R _L = 100 Ω	±10.4	±10.8	V	
			R _L = 30 Ω	±9.9	±10.4		
		V _{CC(H)} = ±15 V	R _L = 100 Ω	±13.3	±13.8	V	
			R _L = 50 Ω	±13	±13.6		
Output voltage transition from V _{CC(L)} to V _{CC(H)} (Point where I _{CC(L)} = I _{CC(H)})		R _L = 50 Ω	V _{CC(L)} = ±5 V	±3.1		V	
			V _{CC(L)} = ±6 V	±3.9			
I _O	Output current (1)	R _L = 10 Ω	V _{CC(H)} = ±12 V	±500		mA	
			V _{CC(H)} = ±15 V	±400	±500		
I _(SC)	Short-circuit current (1)	R _L = 1 Ω	V _{CC(H)} = ±15 V	±750		mA	
Output resistance		Open-loop		5		Ω	
Output resistance—terminate mode		f = 1 MHz,	Gain = +10	0.35		Ω	
Output resistance—shutdown mode		f = 1 MHz,	Open-loop	5.5		kΩ	

(1) A heatsink is required to keep the junction temperature below absolute maximum rating when an output is heavily loaded or shorted. See Absolute Maximum Ratings section for more information.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC(H)} = \pm 15\text{ V}$, $V_{CC(L)} = \pm 5\text{ V}$ $R_F = 1.5\text{ k}\Omega$, Gain = +10, Full Bias Mode, $R_L = 50\ \Omega$ (unless otherwise noted)

POWER SUPPLY								
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$V_{CC(x)}$	Operating range	$\pm V_{CC(H)}$		$\pm V_{CC(L)}$	± 15	± 16.5	V	
		$\pm V_{CC(L)}$		± 3	± 5	$\pm V_{CC(H)}$		
I_{CC}	Quiescent current (each driver) Full-bias mode (Bias-1 = 1, Bias-2 = 1, Bias-3 = X) (I_{CC} trimmed with $V_{CC(H)} = \pm 15\text{ V}$, $V_{CC(L)} = \pm 5\text{ V}$)	$V_{CC(L)} = \pm 5\text{ V};$ ($V_{CC(H)} = \pm 15\text{ V}$)	$T_A = 25^\circ\text{C}$	5.7	6.4	7.5	mA	
			$T_A = \text{full range}$			8.1		
		$V_{CC(L)} = \pm 6\text{ V};$ ($V_{CC(H)} = \pm 15\text{ V}$)	$T_A = 25^\circ\text{C}$		6.7			mA
			$T_A = \text{full range}$					
		$V_{CC(H)} = \pm 12\text{ V};$ ($V_{CC(L)} = \pm 5\text{ V}$)	$T_A = 25^\circ\text{C}$		3.1			mA
			$T_A = \text{full range}$					
		$V_{CC(H)} = \pm 15\text{ V};$ ($V_{CC(L)} = \pm 5\text{ V}$)	$T_A = 25^\circ\text{C}$	2.9	3.25	3.75		mA
			$T_A = \text{full range}$			4.25		
	Quiescent current (each driver) Variable bias modes, $V_{CC(L)} = \pm 5\text{ V}$	Mid; Bias-1 = 1, Bias-2 = 0, Bias-3 = 1			5.0	5.6	6.8	mA
		Low; Bias-1 = 1, Bias-2 = 0, Bias-3 = 0			4.25	4.8	6.0	
		Terminate; Bias-1 = 0, Bias-2 = 1, Bias-3 = X ⁽¹⁾			3.2	3.8	4.5	
		Shutdown; Bias-1 = 0, Bias-2 = 0, Bias-3 = X ⁽¹⁾				1	1.3	
	Quiescent current (each driver) Variable bias modes, $V_{CC(H)} = \pm 15\text{ V}$	Mid; Bias-1 = 1, Bias-2 = 0, Bias-3 = 1			2.4	2.7	3.0	mA
		Low ; Bias-1 = 1, Bias-2 = 0, Bias-3 = 0			1.9	2.15	2.4	
		Terminate; Bias-1 = 0, Bias-2 = 1, Bias-3 = X ⁽¹⁾			1.1	1.3	1.5	
		Shutdown ; Bias-1 = 0, Bias-2 = 0, Bias-3 = X ⁽¹⁾				0.1	0.5	
PSRR	Power supply rejection ratio ($\Delta V_{CC(x)} = \pm 1\text{ V}$)	$V_{CC(L)} = \pm 5\text{ V}$	$T_A = 25^\circ\text{C}$	-70	-82		dB	
			$T_A = \text{full range}$		-68			
		$V_{CC(H)} = \pm 15\text{ V}$	$T_A = 25^\circ\text{C}$	-70	-82			
			$T_A = \text{full range}$		-68			

(1) X is used to denote a logic state of either 1 or 0.

ELECTRICAL CHARACTERISTICS (continued)

 over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC(H)} = \pm 15\text{ V}$, $V_{CC(L)} = \pm 5\text{ V}$, $R_F = 1.5\text{ k}\Omega$, Gain = +10, Full Bias Mode, $R_L = 50\ \Omega$ (unless otherwise noted)

DYNAMIC PERFORMANCE							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BW	Single-ended small-signal bandwidth (-3 dB), $V_O = 0.1\text{ V}_{\text{rms}}$	$R_L = 100\ \Omega$	Gain = +1, $R_F = 750\ \Omega$		80		MHz
			Gain = +2, $R_F = 620\ \Omega$		70		
			Gain = +5, $R_F = 500\ \Omega$		60		
			Gain = +10, $R_F = 1\text{ k}\Omega$		20		
		$R_L = 25\ \Omega$	Gain = +1, $R_F = 750\ \Omega$		60		MHz
			Gain = +2, $R_F = 620\ \Omega$		55		
			Gain = +5, $R_F = 500\ \Omega$		50		
			Gain = +10, $R_F = 1\text{ k}\Omega$		17		
SR	Single-ended slew-rate ⁽¹⁾	$V_O = 20\text{ V}_{\text{pp}}$, Gain = +10			300		V/ μs

(1) Slew-rate is defined from the 25% to the 75% output levels

DC PERFORMANCE							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	$V_{CC(L)} = \pm 5\text{ V}, \pm 6\text{ V}$	$T_A = 25^\circ\text{C}$		1	15	mV
			$T_A = \text{full range}$			20	
	Differential offset voltage		$T_A = 25^\circ\text{C}$		0.3	6	
			$T_A = \text{full range}$			8	
	Offset drift		$T_A = \text{full range}$		40		$\mu\text{V}/^\circ\text{C}$
I_{IB}	-Input bias current	$V_{CC(L)} = \pm 5\text{ V}, \pm 6\text{ V}$	$T_A = 25^\circ\text{C}$		1	15	μA
			$T_A = \text{full range}$			20	
	+ Input bias current		$T_A = 25^\circ\text{C}$		1.5	15	
			$T_A = \text{full range}$			20	
Z_{OL}	Open loop transimpedance	$R_L = 1\text{ k}\Omega$			2		M Ω

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC(H)} = \pm 15\text{ V}$, $V_{CC(L)} = \pm 5\text{ V}$ $R_F = 1.5\text{ k}\Omega$, Gain = +10, Full Bias Mode, $R_L = 50\ \Omega$ (unless otherwise noted)

INPUT CHARACTERISTICS							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ICR}	Input common-mode voltage range(1)	$V_{CC(L)} = \pm 5\text{ V}$	$T_A = 25^\circ\text{C}$	± 2.7	± 3.0	V	
			$T_A = \text{full range}$	± 2.6			
		$V_{CC(L)} = \pm 6\text{ V}$	$T_A = 25^\circ\text{C}$		± 4.0		
REF pin input voltage range	$V_{CC-(L)} = \pm 5\text{ V}$			± 2.5	V		
	$V_{CC(L)} = \pm 6\text{ V}$			± 3.5			
CMRR	Common-mode rejection ratio	$V_{CC(L)} = \pm 5\text{ V}, \pm 6\text{ V}$	$T_A = 25^\circ\text{C}$	60	67	dB	
			$T_A = \text{full range}$	57			
R_I	Input resistance	+ Input			800	$\text{k}\Omega$	
		- Input			45	Ω	
C_I	Differential Input capacitance				1.2	pF	

(1) To conserve as much power as possible, the input stage of the THS6132 is powered from the $V_{CC(L)}$ supplies and is limited by the $V_{CC(L)}$ supply voltage. For Class-AB operation, connect the $V_{CC(L)}$ supplies to $V_{CC(H)}$.

LOGIC CONTROL CHARACTERISTICS							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	Bias pin voltage for logic 1	Relative to DGND pin voltage		2.0			V
V_{IL}	Bias pin voltage for logic 0	Relative to DGND pin voltage				0.8	V
I_{IH}	Bias pin current for logic 1	$V_{IH} = 5\text{ V}, \text{ DGND} = 0\text{ V}$		-0.1		-0.2	μA
I_{IL}	Bias pin current for logic 0	$V_{IL} = 0\text{ V}, \text{ DGND} = 0\text{ V}$		-0.1		-0.2	μA
	Transition time—logic 0 to logic 1(1)				0.1		μs
	Transition time—logic 1 to logic 0(1)				0.2		μs
	DGND useable range			$-V_{CC(H)}$		$+V_{CC(H)} - 5$	V

(1) Transition time is defined as the time from when the logic signal is applied to the time when the supply current has reached half its final value.

LOGIC TABLE					
BIAS-1	BIAS-2	BIAS-3	FUNCTION	DESCRIPTION	
1	1	X(1)	Full bias mode	Amplifiers ON with lowest distortion possible	
1	0	1	Mid bias mode	Amplifiers ON with power savings with a reduction in distortion performance	
1	0	0	Low bias mode	Amplifiers ON with enhanced power savings and a reduction of distortion performance	
0	1	X(1)	Terminate mode	Lowest power state with +Vin pins internally connect to REF pin and output has low impedance	
0	0	X(1)	Shutdown mode	Amplifiers OFF and output has high impedance	

(1) X is used to denote a logic state of either 1 or 0.

NOTE: The default state for all logic pins is a logic one (1).

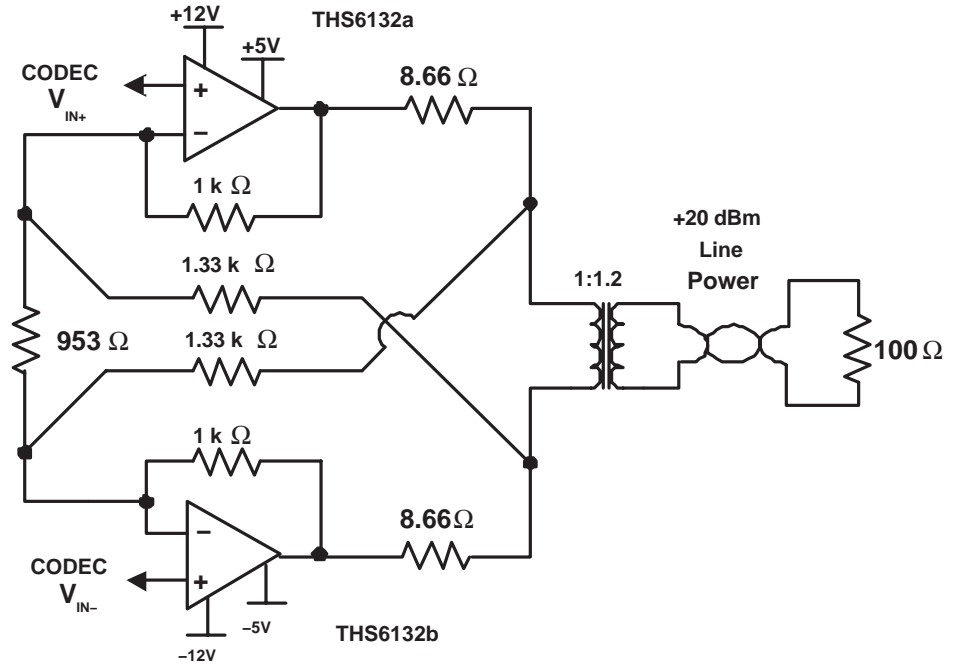
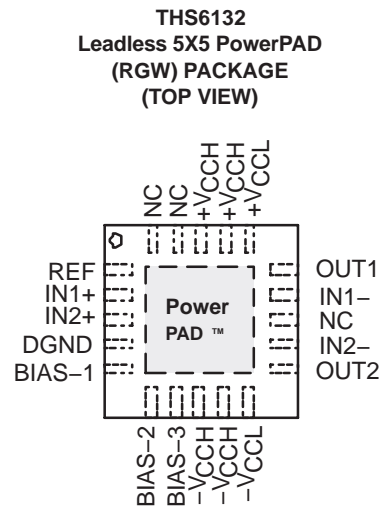
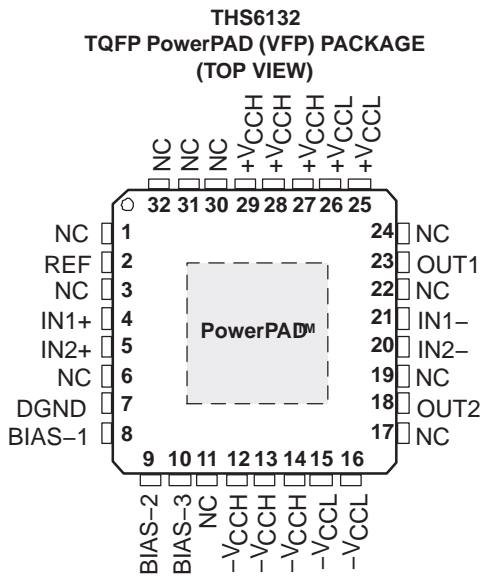


Figure 1. ± 12 V Active Termination ADSL CO Line Driver Circuit (Synthesis Factor = 4; CF = 5.6)

PIN ASSIGNMENTS



TYPICAL CHARACTERISTICS

Table of Graphs

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OUTPUT VOLTAGE HEADROOM
vs
OUTPUT CURRENT

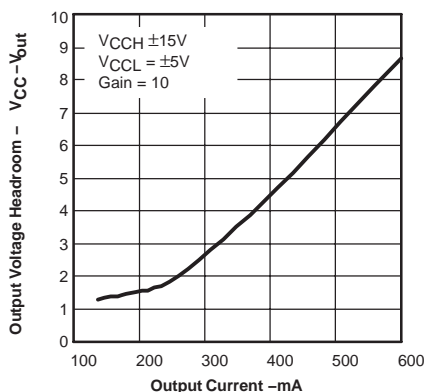


Figure 2

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

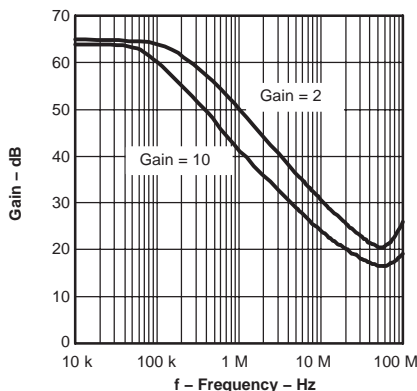


Figure 3

CROSSTALK
vs
FREQUENCY

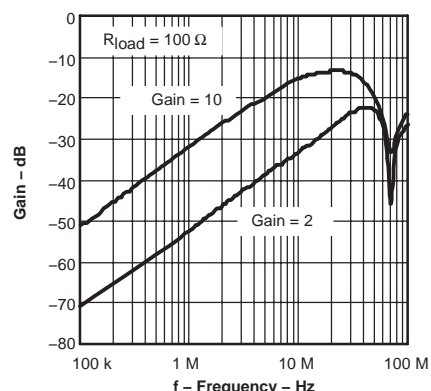


Figure 4

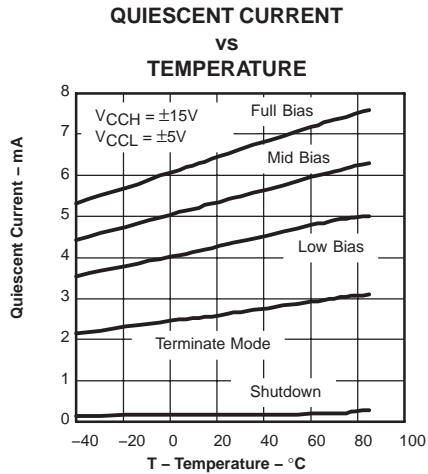


Figure 5

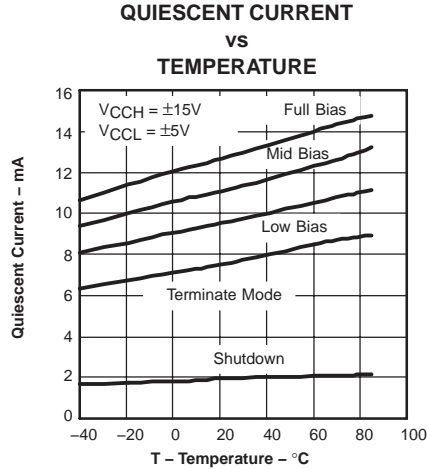


Figure 6

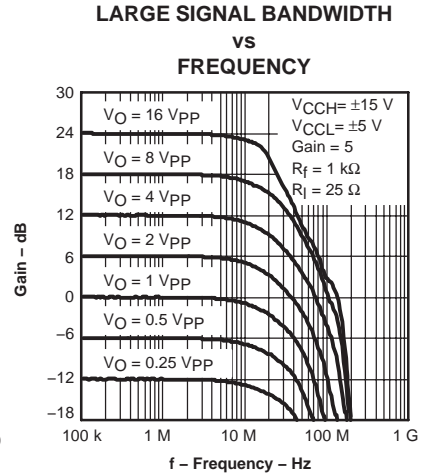


Figure 7

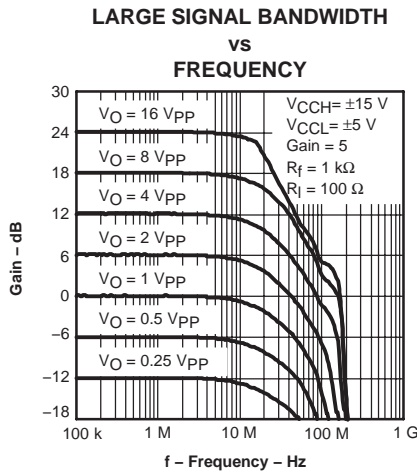


Figure 8

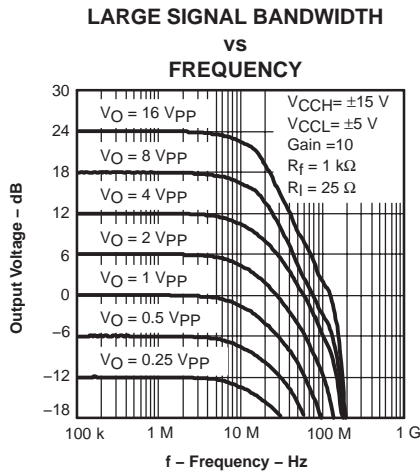


Figure 9

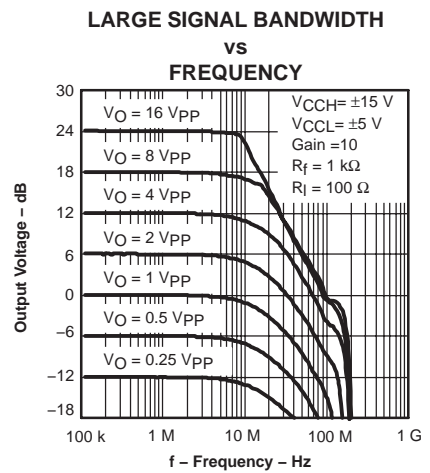


Figure 10

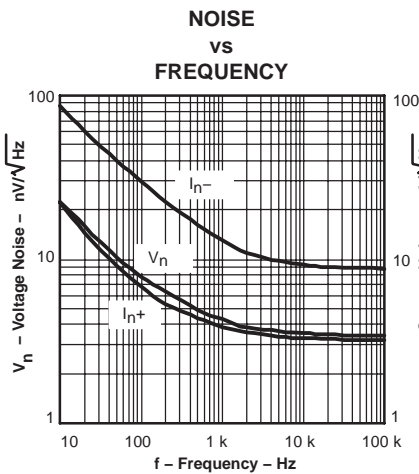


Figure 11

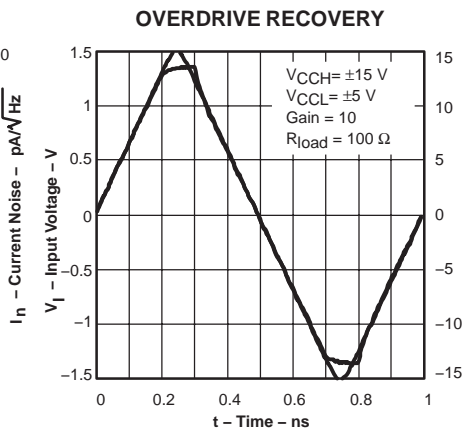


Figure 12

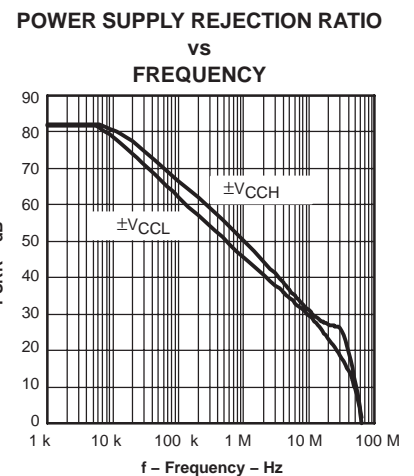


Figure 13

SMALL SIGNAL FREQUENCY RESPONSE

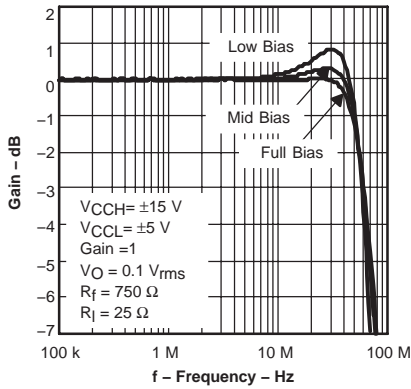


Figure 14

SMALL SIGNAL FREQUENCY RESPONSE

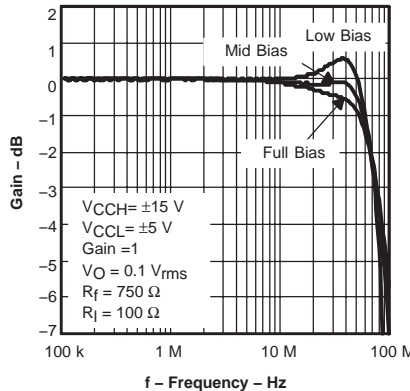


Figure 15

SMALL SIGNAL FREQUENCY RESPONSE

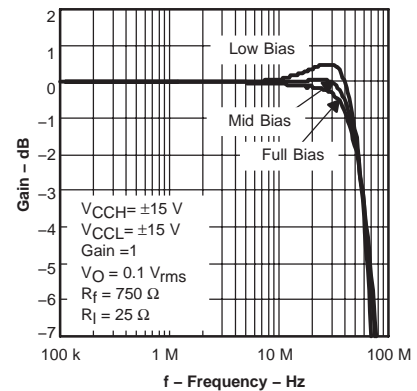


Figure 16

SMALL SIGNAL BANDWIDTH
vs
FREQUENCY

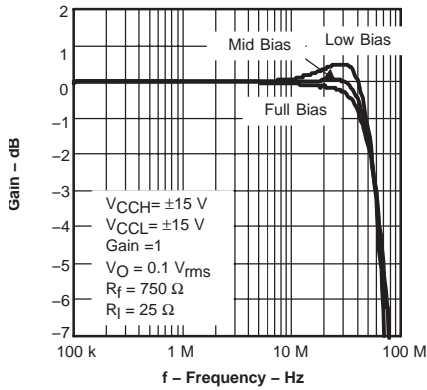


Figure 17

SMALL SIGNAL BANDWIDTH
vs
FREQUENCY

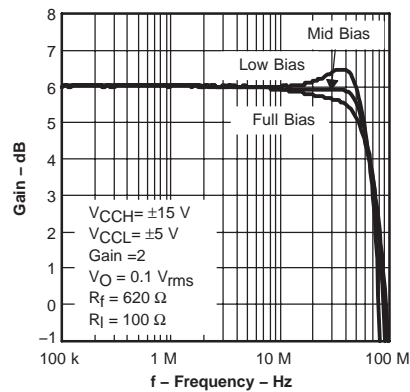


Figure 18

SMALL SIGNAL BANDWIDTH
vs
FREQUENCY

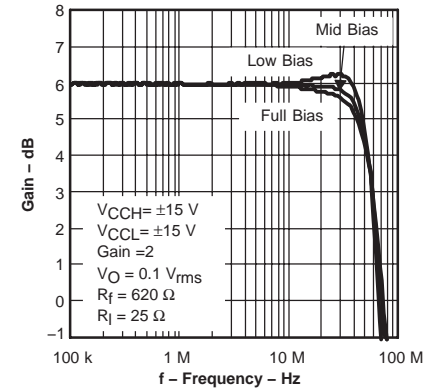


Figure 19

SMALL SIGNAL BANDWIDTH
vs
FREQUENCY

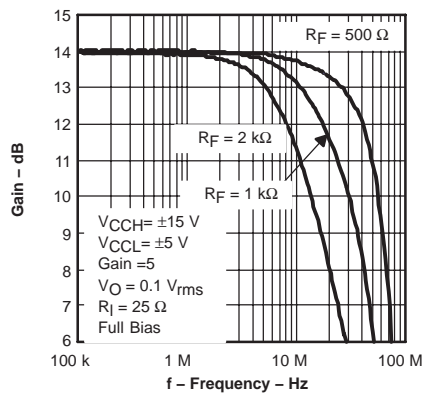


Figure 20

SMALL SIGNAL BANDWIDTH
vs
FREQUENCY

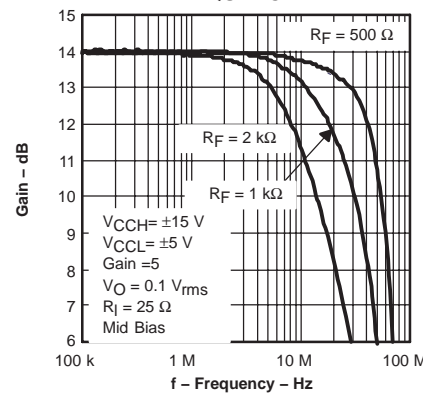


Figure 21

SMALL SIGNAL BANDWIDTH
vs
FREQUENCY

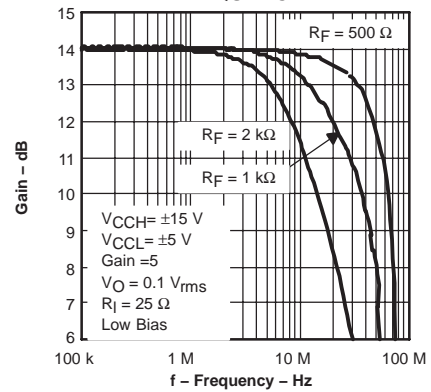


Figure 22

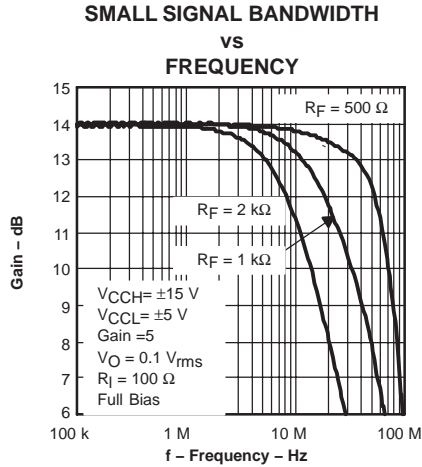


Figure 23

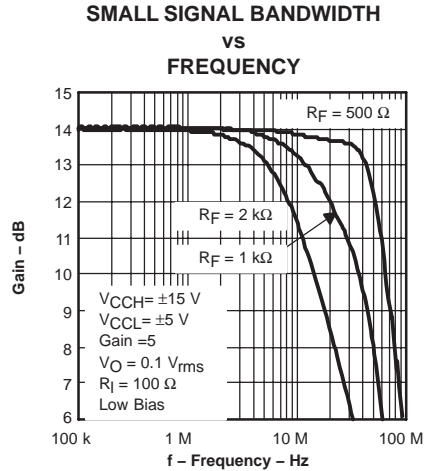


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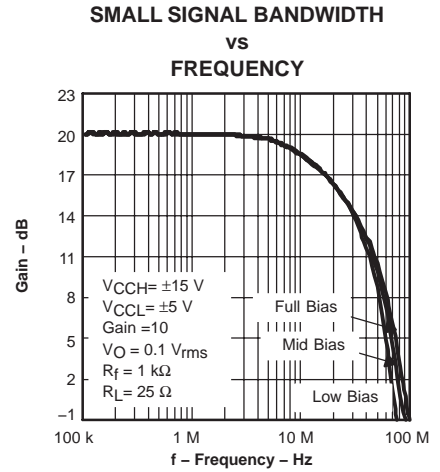


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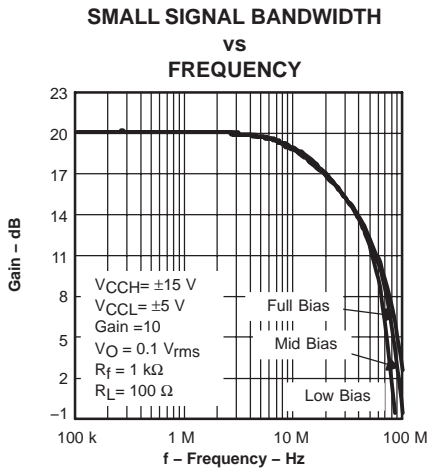


Figure 26

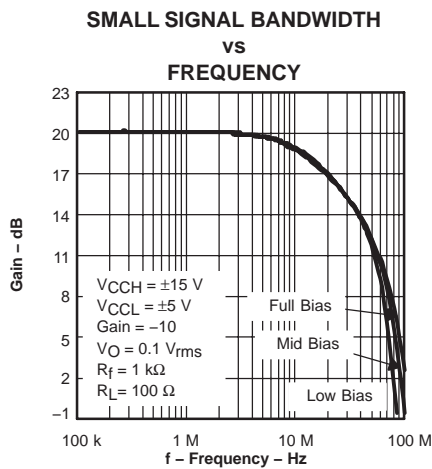


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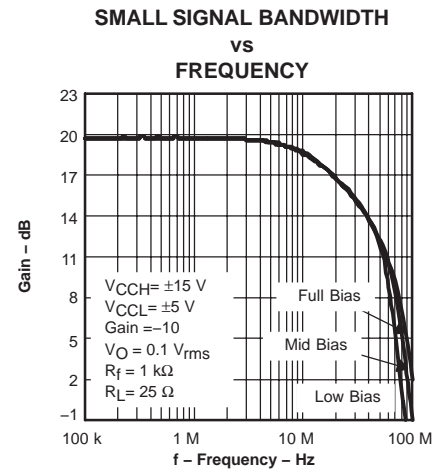


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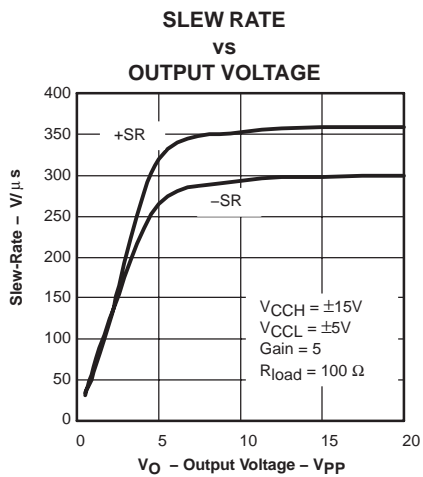


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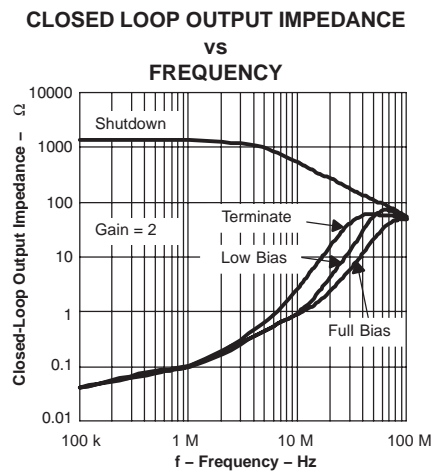


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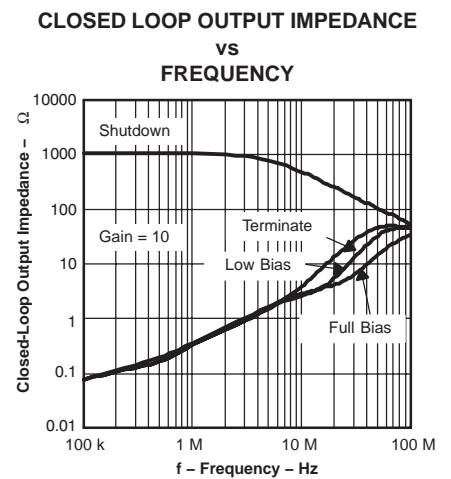


Figure 31

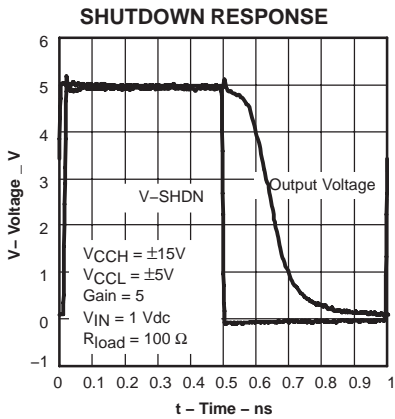


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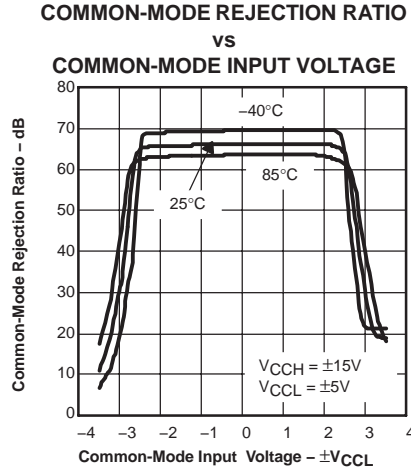


Figure 33

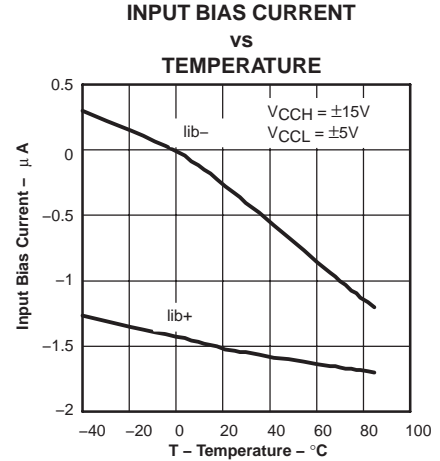


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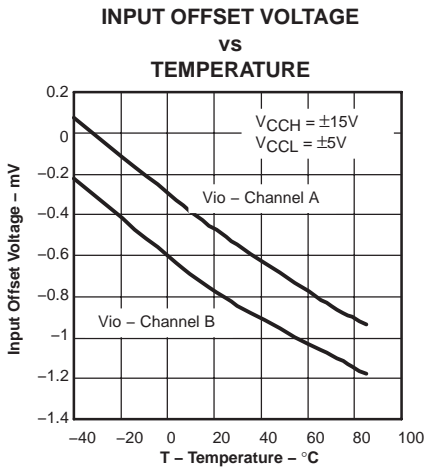


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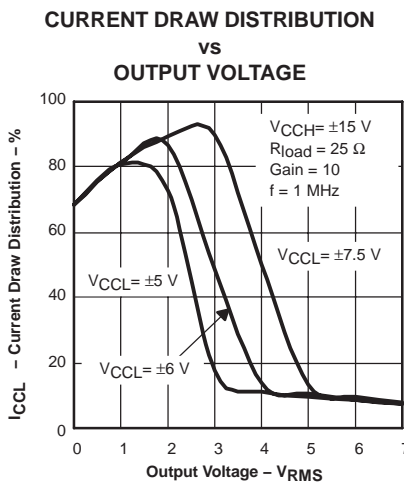


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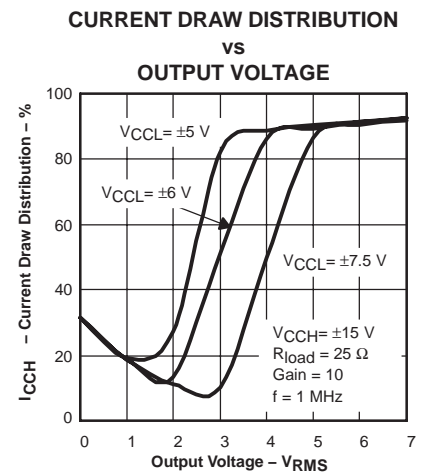


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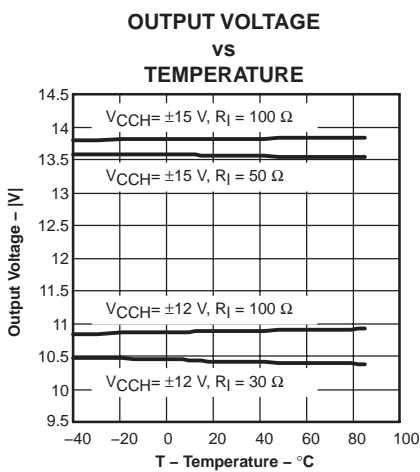


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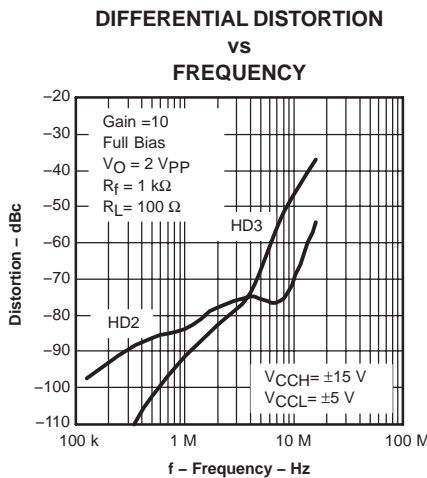


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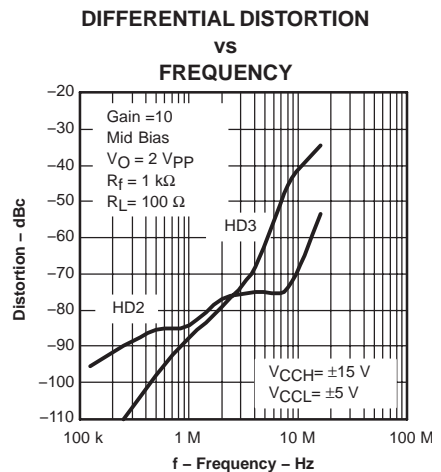


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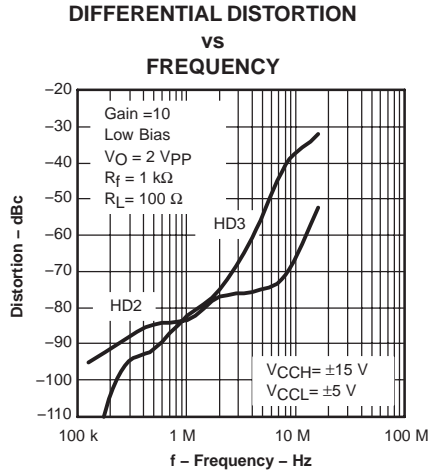


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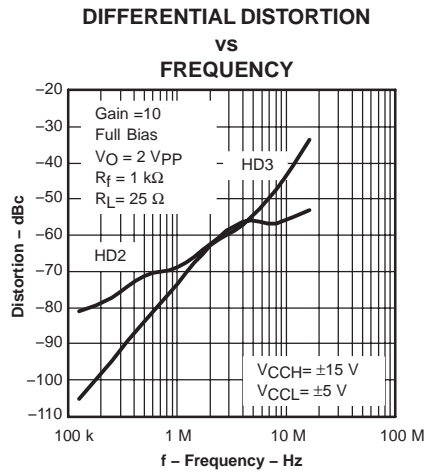


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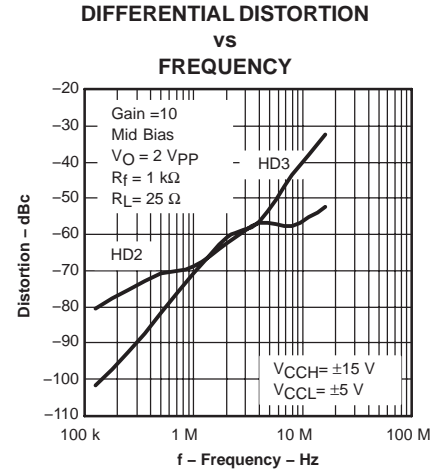


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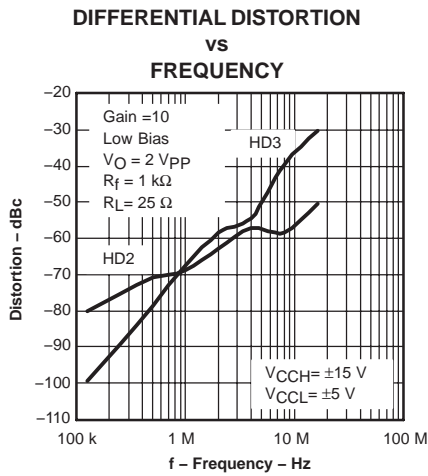


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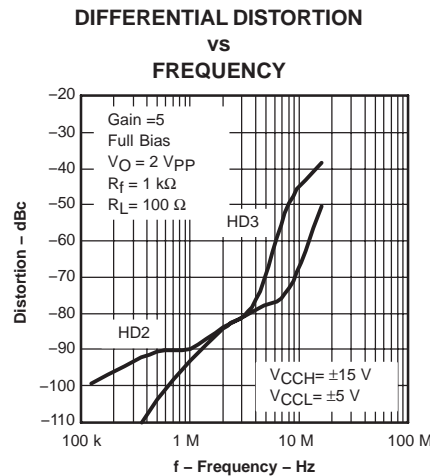


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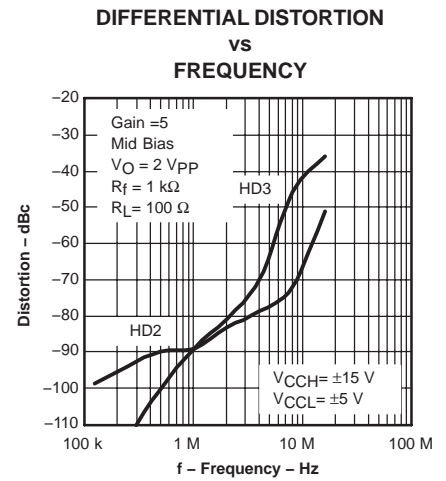


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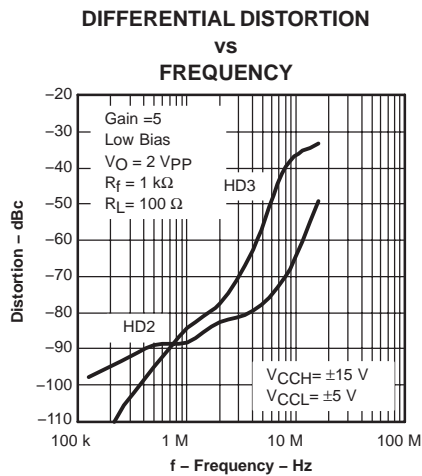


Figure 47

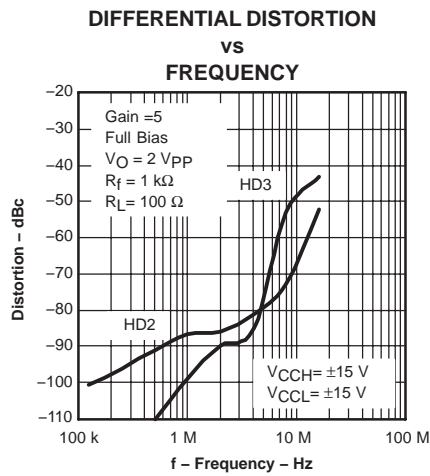


Figure 48

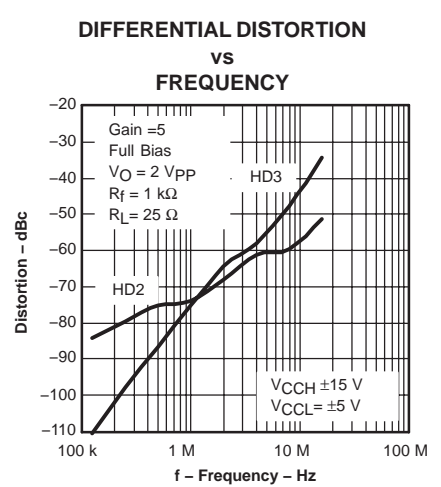


Figure 49

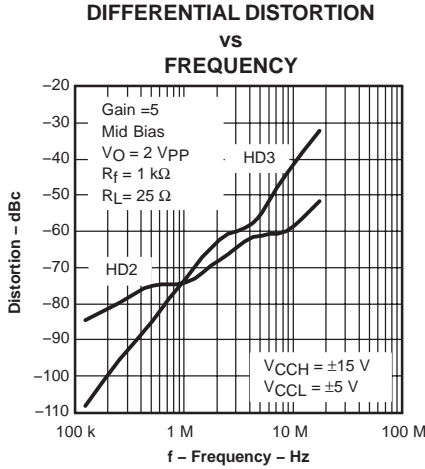


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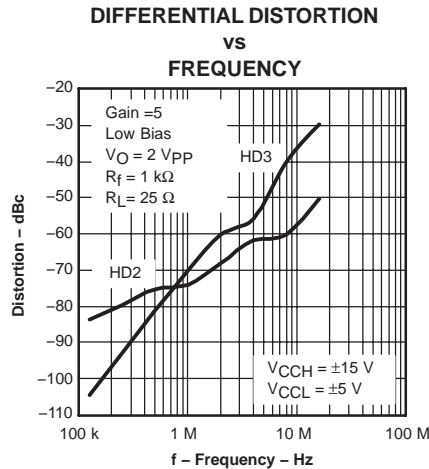


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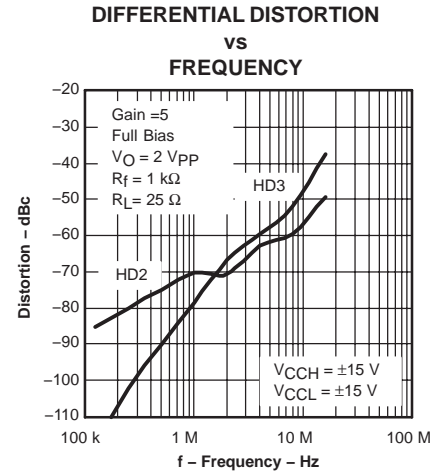


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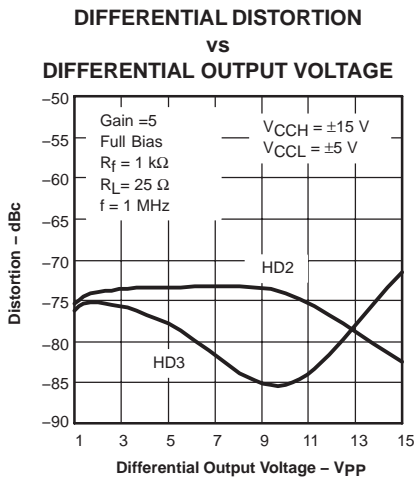


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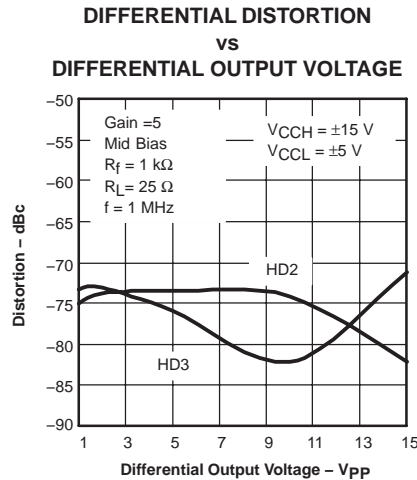


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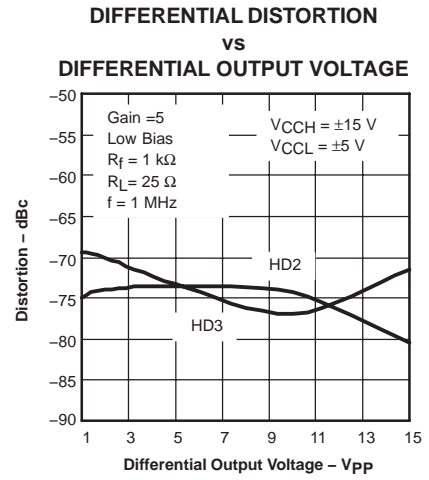


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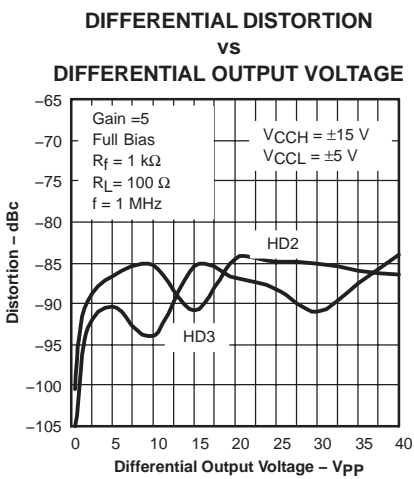


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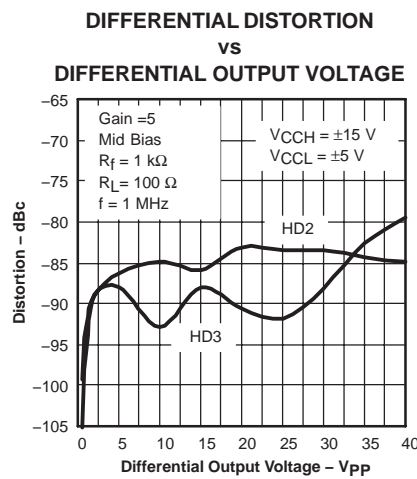


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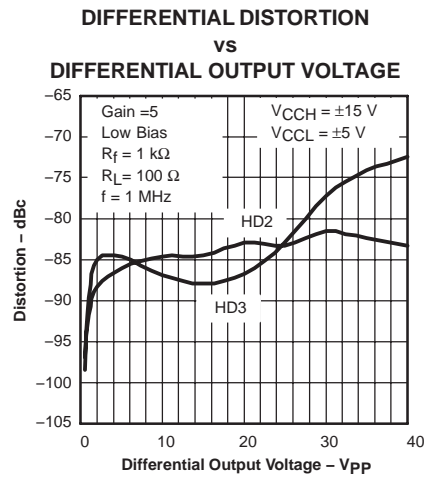


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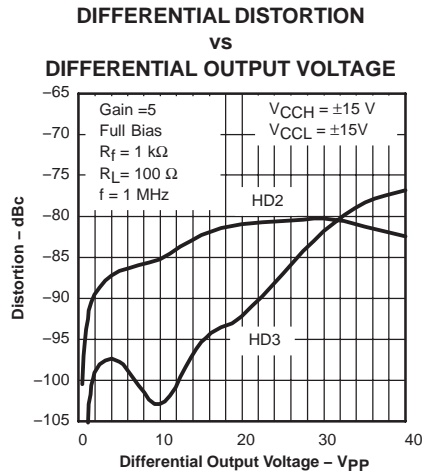


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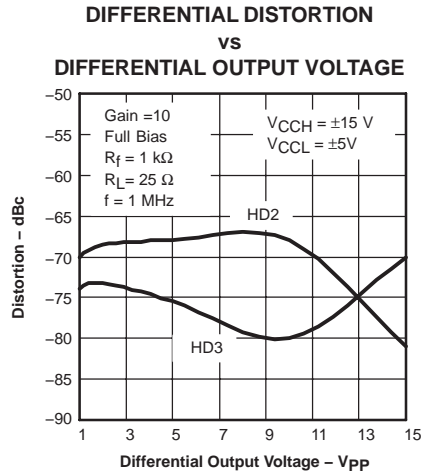


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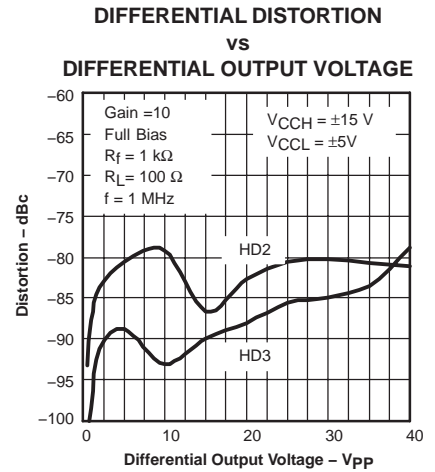


Figure 61

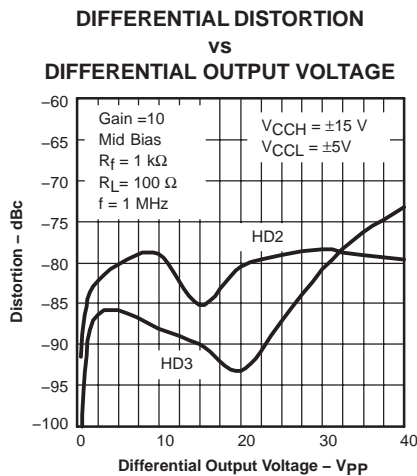


Figure 62

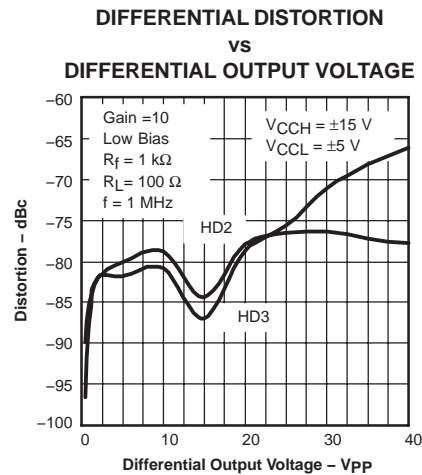


Figure 63

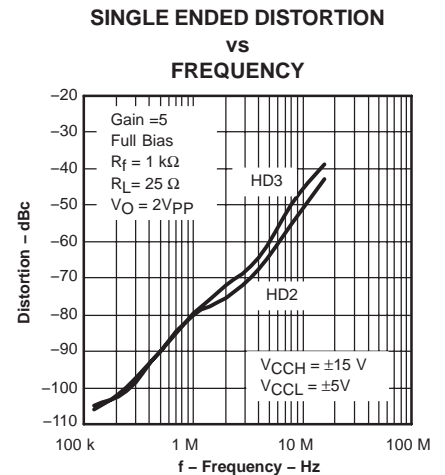


Figure 64

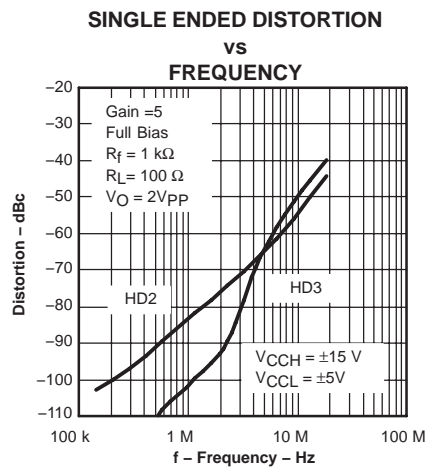


Figure 65

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
THS6132RGWR	ACTIVE	QFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6132RGWRG4	ACTIVE	QFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6132VFP	ACTIVE	HLQFP	VFP	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6132VFPG4	ACTIVE	HLQFP	VFP	32		TBD	Call TI	Call TI
THS6132VFPR	ACTIVE	HLQFP	VFP	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS6132VFPRG4	ACTIVE	HLQFP	VFP	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6132RGWR	QFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
THS6132VFPR	HLQFP	VFP	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

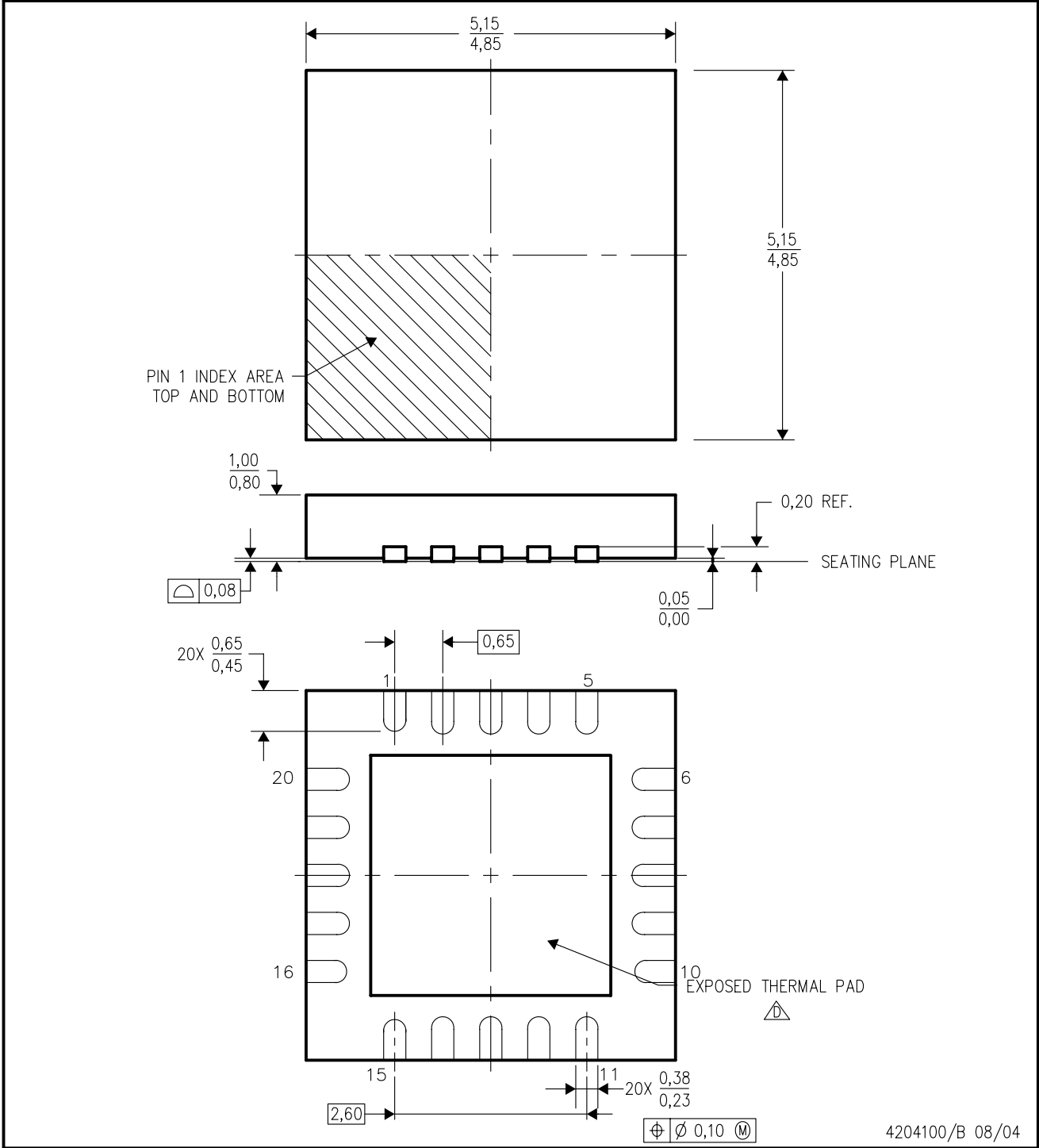


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6132RGWR	QFN	RGW	20	3000	340.5	333.0	20.6
THS6132VFPR	HLQFP	VFP	32	1000	346.0	346.0	33.0

RGW (S-PQFP-N20)

PLASTIC QUAD FLATPACK



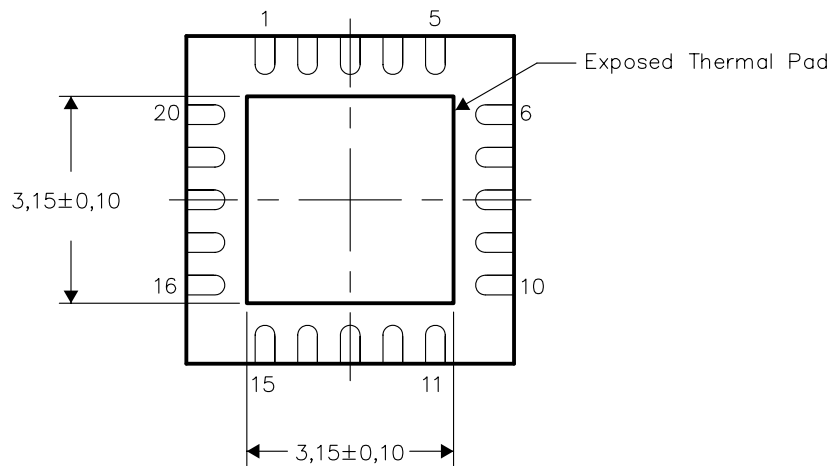
- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
- B. This drawing is subject to change without notice.
- C. Quad Flat pack, No-leads (QFN) package configuration
- △ The package thermal pad must be soldered to the board for thermal and mechanical performance.. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

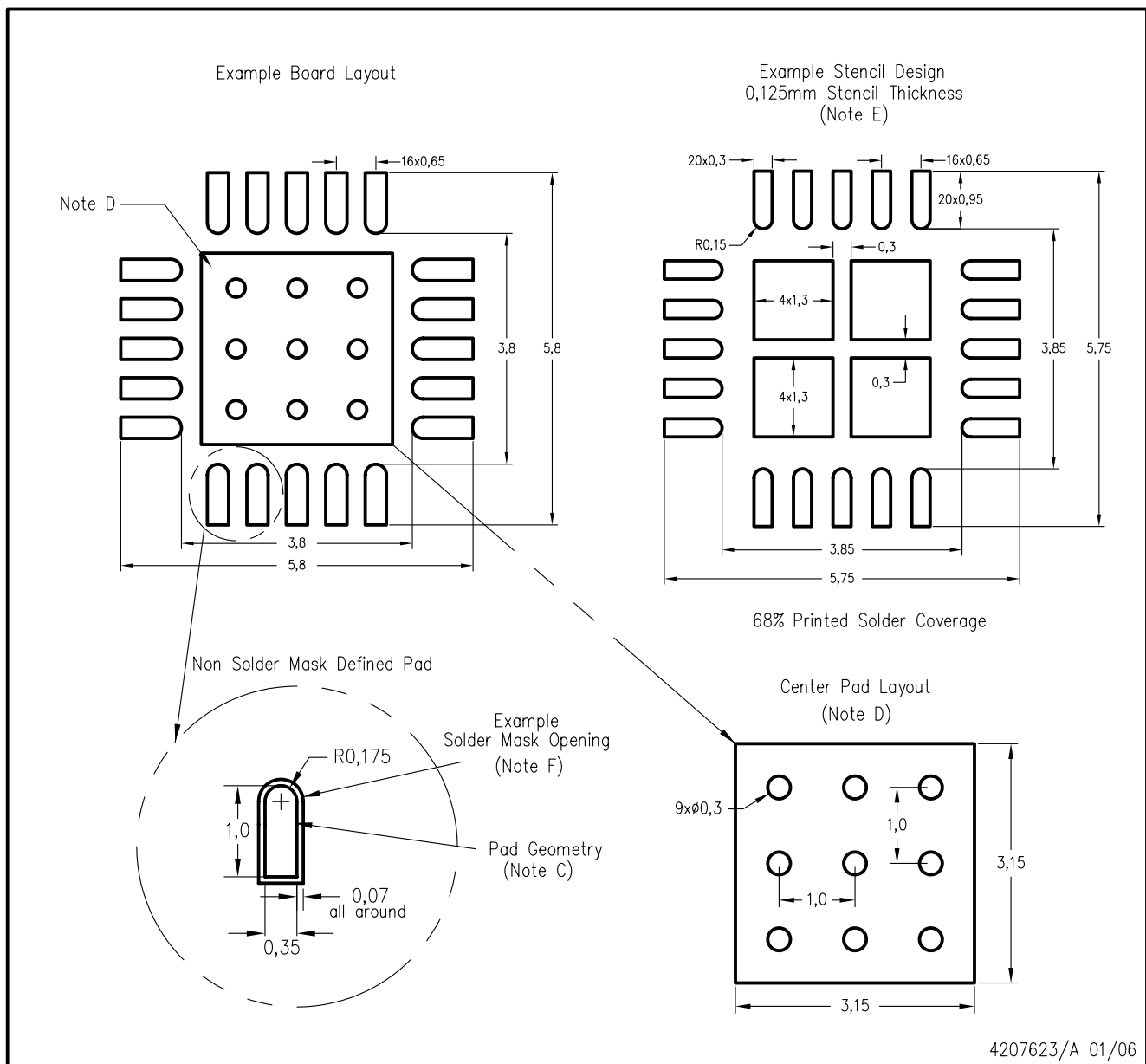


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGW (S-PQFP-N20)

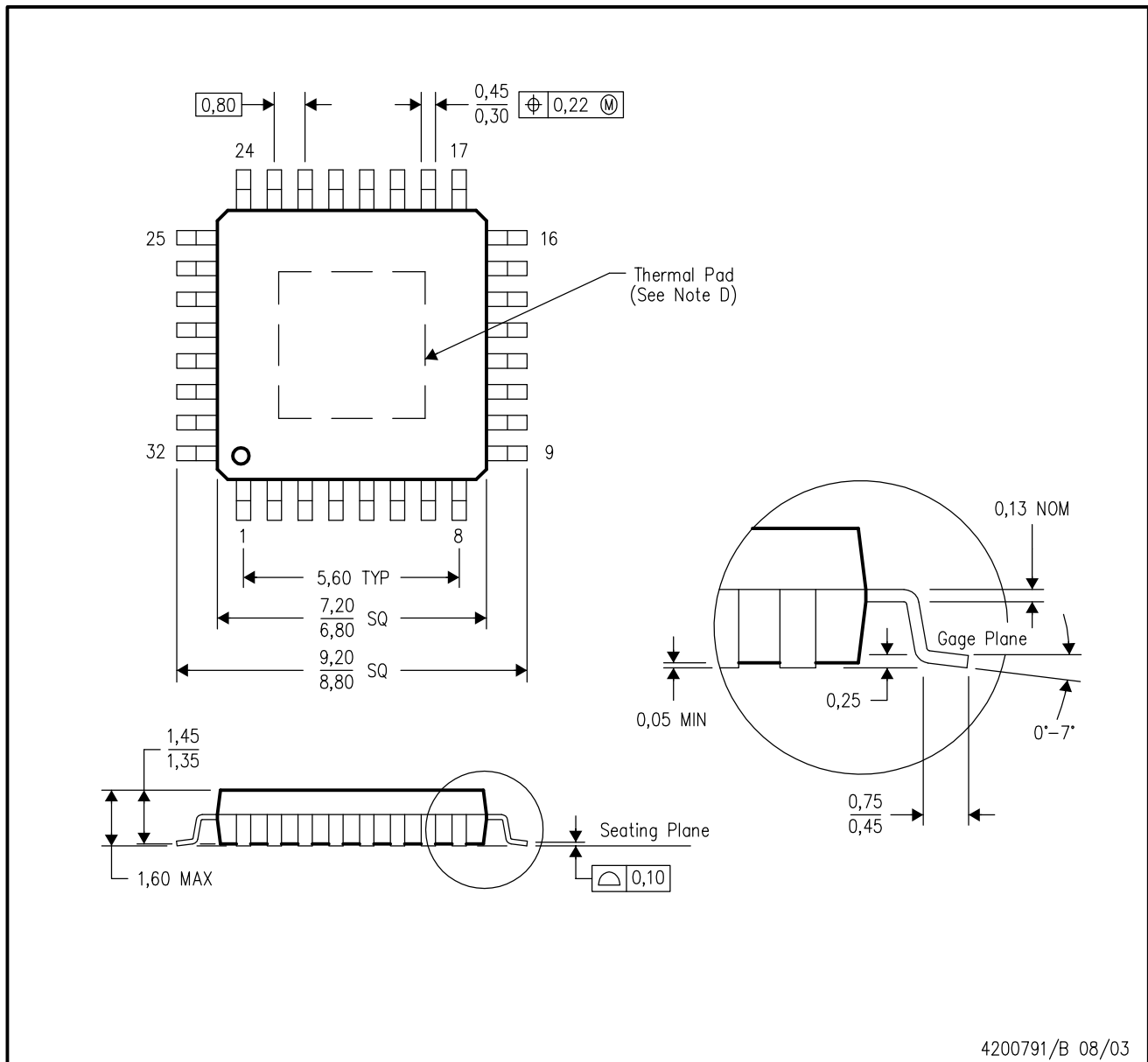


4207623/A 01/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

VFP (S-PQFP-G32)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. Falls within JEDEC MS-026
 - F. PowerPAD is a trademark of Texas Instruments Incorporated.

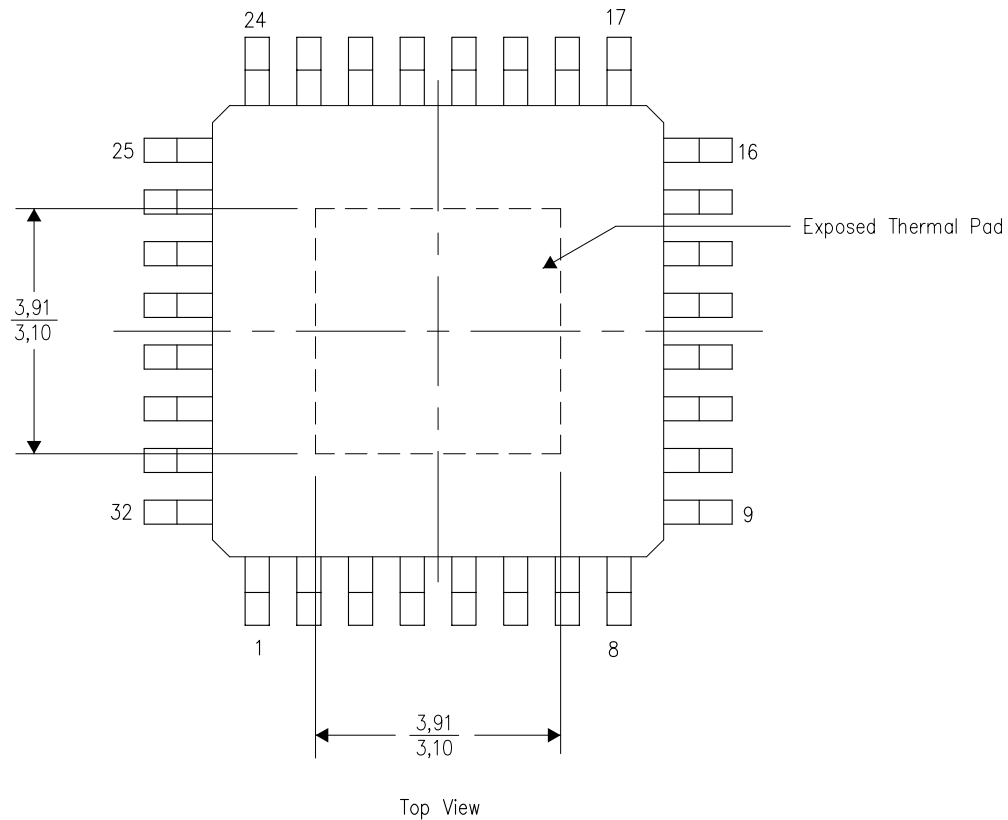
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

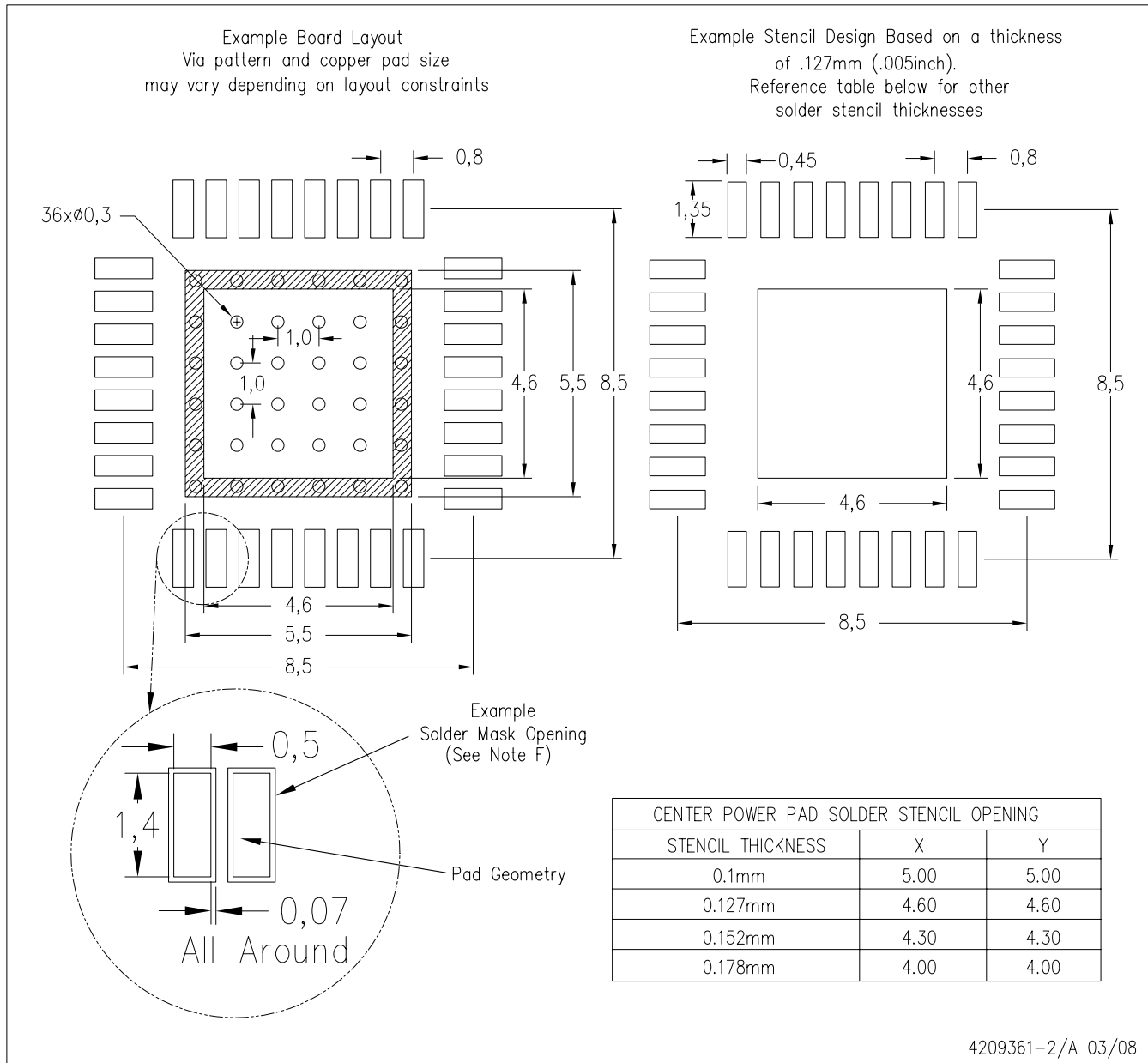
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

VFP (S-PQFP-G32) PowerPAD™



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

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